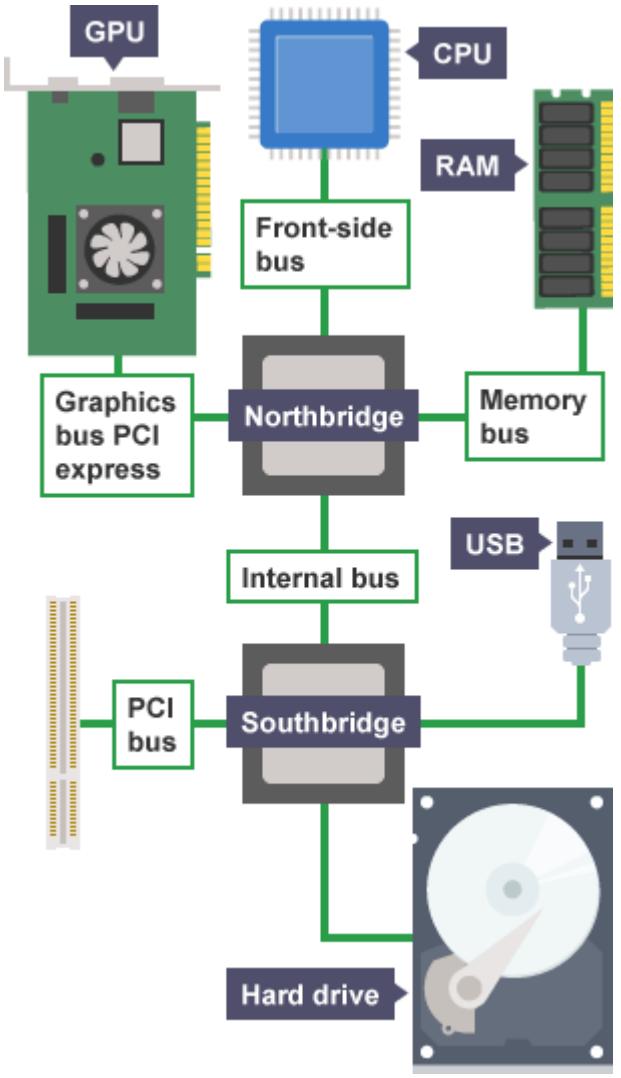
Computing GCSE – 1.1

J276/01 – Systems Architecture A

KEY VOCABULARY	
CPU	*Central Processing Unit*. - The "brain" of the computer
CU	*Control Unit.* - Part of the CPU that manages the functions of all other parts of the CPU
Decoder	Part of the CU which decodes the binary instructions fetched from memory
RAM	*Random Access Memory* - The main volatile memory into which programs are loaded from the hard drive
MAR	*Memory Address Register* - Small fast memory used to store the RAM address of the next instruction
MDR	*Memory Data Register* - Small, fast memory used to store the information collected from the RAM before processing
PC	*Program Counter* - Keeps track of the current instruction number of the program
Accumulator	Small, fast memory, used to keep track of the data currently being processed
ALU	*Arithmetic and Logic Unit* - Does the basic mathematics and comparisons during processing
Bus	A physical connection between two elements of a computer system that allows the transfer of data.
Cache	Incredibly fast, but very expensive volatile memory using in the CPU
Bridge (North / South)	Junctions on a motherboard where the bus connections are controlled and routed. Northbridge deals with core functions, whilst the Southbridge deals with the peripherals, input and output devices and Secondary Storage.
von Neumann Architecture	The method used by all modern computers to allow the programming of a machine to be changed depending on the required function.
Fetch / Decode / Execute Cycle	Basis of the von Neumann architecture – the repeated process where instructions are fetched from RAM, decoded into tasks and data, then carried out.
Clock Speed	The number of FDE cycles that a CPU can carry out per second. Measured in Ghz (1 Ghz = 10^9 cycles per second or 1,000,000,000hz)
Cores	Some processors have multiple CPUs which can work in parallel, sequentially or can multitask. Dual and Quad cores are common in modern PCs

An example of a typical PC's innards.



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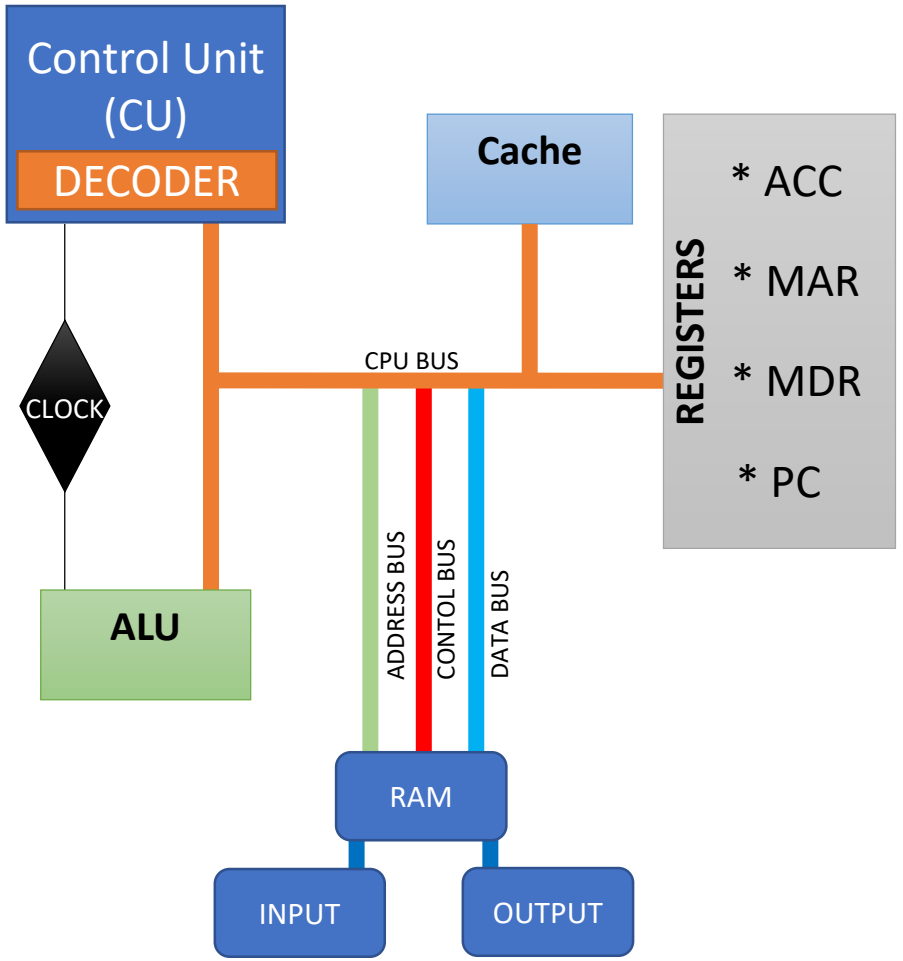
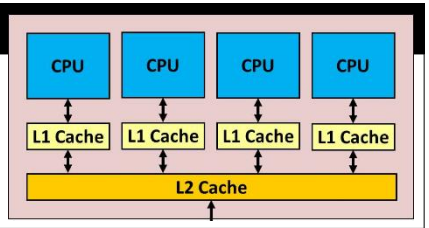
J276/01 – Systems Architecture B

BASIC DIAGRAM OF CPU

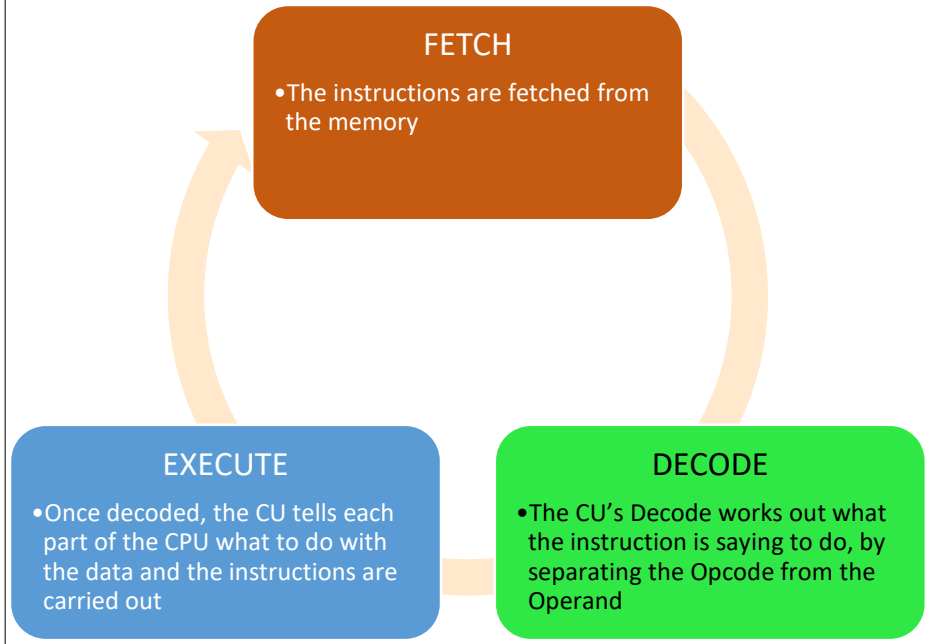


Multi Core Processing

Some processors have multiple CPU cores on one chip. They all have their own Level 1 cache, but share Level 2 cache, allowing them to collaborate quickly on large tasks.

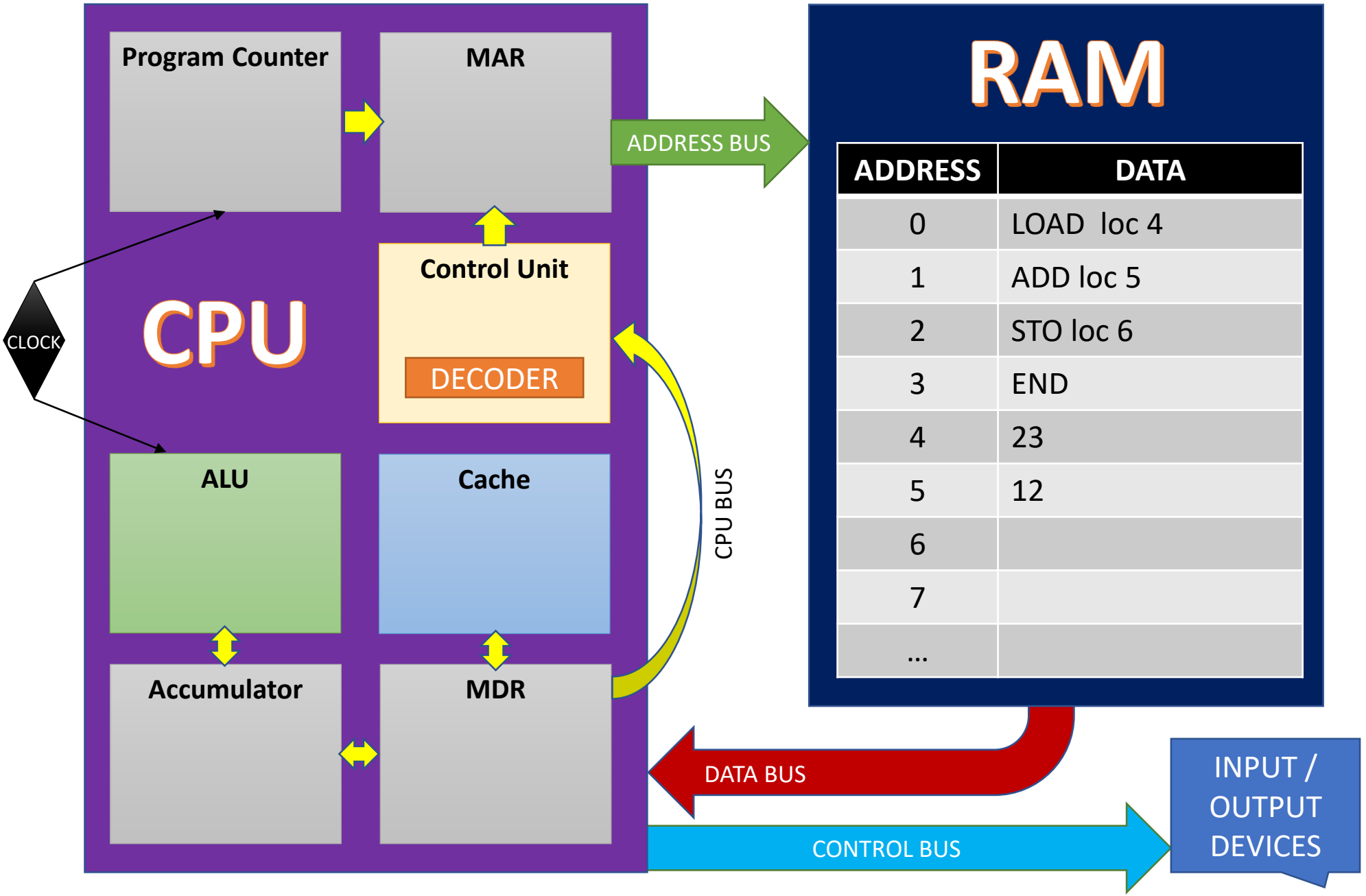


The FETCH – DECODE – EXECUTE cycle



KEY VOCABULARY

Machine Code	A program, stored in binary, that the CPU undertakes the FDE cycle on. All programs must be in machine code to work
Instruction	A single line of machine code, containing the command and data location on which it is to be executed. Stored in binary
Opcode	The first part of the instruction, is the command
Operand	The second part of the instruction is the data on which to carry out the command. This may be actual data stored in binary form, or a memory location reference of where to find the data


Program Counter
MAR
ADDRESS BUS
RAM
ADDRESS
DATA
0
LOAD loc 4
1
ADD loc 5
2
STO loc 6
3
END
4
23
5
12
6
7
...
Control Unit
CPU
DECODER
CLOCK
ALU
Cache
CPU BUS
Accumulator
MDR
DATA BUS
CONTROL BUS
INPUT / OUTPUT DEVICES